IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.; AVNET, INC.,** Defendants.	)	Case No. 2:25-cv-557-JRG JURY TRIAL DEMANDED (Lead Case)
NETLIST, INC. Plaintiff, v. **MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., MICRON TECHNOLOGY TEXAS LLC; AVNET, INC.,** Defendants.	)	Case No. 2:25-cv-558-JRG JURY TRIAL DEMANDED (Member Case)

FIRST AMENDED COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, brings this First Amended Complaint against defendants Micron Technology Inc. ("Micron Technology"), Micron Semiconductor Products, Inc. ("Micron Semiconductor"), and Micron Technology Texas, LLC ("Micron Texas") (collectively, "Micron") and Avnet, Inc. ("Avnet") (collectively, "Defendants") for infringement of U.S. Patent Nos. 12,308,087 ("the '087 Patent," Ex. 1) and 10,025,731 ("the '731 Patent," Ex. 2).

2. Micron has also filed a series of retaliatory suits in its home state of Idaho, accusing Netlist of bad faith assertion of certain other Netlist patents under Idaho Code § 48-1703. *See Netlist, Inc. v. Micron Technology, Inc.*, No. 2:23-cv-628, Dkt. 1 ¶¶ 20-27; Dkt. 14 ¶¶ 23-31 (summarizing Micron's pattern of filing retaliatory suits). It is only a matter of time before Micron brings another similar suit in Idaho state court on the '087 and '731 Patents. Therefore, Netlist seeks a declaration that this suit was not brought in bad faith; a declaration that Netlist has not made bad faith assertion of patent infringement under Idaho Code § 48-1703; and a declaration that Defendants are not entitled to relief under Idaho Code § 48-1703.

I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Way, Suite 100, Irvine, CA 92617.

4. On information and belief, Micron makes dynamic random-access memory ("DRAM"), NAND Flash, and NOR Flash memory, and other memory products in semiconductor fabrication plants in the United States and other countries throughout the world. On information and belief, Micron sells its products, either directly or through distributors, retailers, authorized dealers, and sales agents, including Avnet, Inc. (Ex. 13), to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives and mobile telecommunications markets.

5. On information and belief, Micron Technology is a corporation organized and existing under the laws of Delaware. On information and belief, Micron Technology has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Technology is registered to do business in the State of Texas,

and can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

6. On information and belief, Micron Semiconductor is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Semiconductor has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Semiconductor can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701-3218.

7. On information and belief, Micron Texas is a corporation organized and existing under the laws of Idaho. On information and belief, Micron Texas has a regular and established place of business at 805 Central Expressway South, Suite 100, Allen, Texas 75013. On information and belief, Micron Texas also has a regular and established place of business at 950 West Bethany Drive, Suite 120, Allen, Texas 75013-3837. On information and belief, Micron Texas is registered with the Texas Secretary of State to do business in Texas. On information and belief, Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

8. On information and belief, Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. On information and belief, Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

9. On information and belief, Avnet is a corporation organized and existing under the laws of New York. On information and belief, Avnet is involved in the use, offering for sale and/or

sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, Avnet has a regular and established place of business at 3101 E. President George Bush Highway, Suite 250, Richardson, TX 75082. On information and belief, Avnet is registered with the Texas Secretary of State to do business in Texas. On information and belief, Avnet can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

10. On information and belief, Defendants have semiconductor fabrication plants in the United States and other countries throughout the world and manufacture memory products such as DRAM, NAND Flash, and NOR Flash at those plants. On information and belief, Defendants also use, sell, and offer for sale in the United States, import into the United States and/or export from the United States memory products, including DDR5 dual in-line memory modules ("DIMMs"). On information and belief, Defendants have at least used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district, *e.g.*, through sales and distribution channels managed by Micron Texas.

11. On information and belief, Defendants place, have placed, and contributed to placing Accused Instrumentalities into the stream of commerce via an established distribution channel knowing or understanding that such products would be sold and used in the United States, including in this judicial district. On information and belief, Defendants have also derived substantial revenues from infringing acts in this judicial district, including from the sale and use of the Accused Instrumentalities.

12. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

13. The Court has subject matter jurisdiction under 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

14. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

15. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, ships, distributes, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce, both directly and through intermediaries (including distributors, retailers, authorized dealers, sales agents, and other individuals or entities), knowing or understanding that such products would be sold and used in the United States, including in this District.

16. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b) because Defendants (1) have committed and continue to commit acts of patent infringement in this District by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that infringe one or more claims of the Patents-in-Suits, including through distributors, retailers, authorized dealers, and sales agents in Texas and this Judicial District, including Avnet (Ex. 13), and (2) have done and continue to do business in this District by maintaining regular and established places of business, including at least at 805 Central Expressway South, Suite 100, Allen, Texas 75013.

17. Venue is also proper for Avnet because it maintains a regular and established place of business in this judicial district at 3101 E. President George Bush Highway, Suite 250, Richardson, TX 75082 and has committed acts of infringement in this judicial district. Specifically, Avnet offers for sale and distributes its products, including the Accused Instrumentalities supplied by Micron, all throughout the United States, including the State of Texas and the Eastern District of Texas. Ex. 13. Avnet's website, https://www.avnet.com/americas/, has an (800) contact number that prospective customers can call to obtain more information or a quote for the Accused Instrumentalities (and other products). Avnet's website also specifically targets customers in Texas, including those in the Eastern District of Texas, by providing region-specific email contact, including dallas@avnet.com. Avnet has been an official distributor for Micron for more than 40 years, "helping [Micron's] customers to innovate and win." Ex. 15. In addition to offering for sale, selling, and distributing the Accused Instrumentalities as Micron's official distributor, "Avnet and Micron also work cooperatively to train engineers on design techniques to leverage next-generation memory technologies." *Id*.

18. Therefore, Micron, together with Avnet as a distributor of the Accused Instrumentalities, have offered to sell, have sold, and have intentionally and voluntarily placed infringing products into the stream of commerce with the expectation and understanding that those products will be sold, purchased, and/or used by its customers in the State of Texas, including the Eastern District of Texas.

III. FACTUAL ALLEGATIONS

A. Background

19. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance

computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase. Netlist has secured multiple jury verdicts confirming the commercial success of its inventions. For example, in 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist $303.15 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:21-cv-463, Dkt. 479. As another example, in May 2024, a jury in the Eastern District of Texas awarded Netlist $445 million in damages against Micron. *See Netlist, Inc. v. Micron Technology Texas, LLC*, No. 2:22-cv-294, Dkt. 135. And in November 2024, a jury found that Samsung willfully infringed three other Netlist patents and awarded Netlist $118 million in damages. *See Netlist, Inc. v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-293, Dkt. 847.

20. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. Netlist's pioneering NVDIMM products utilized the same on-module power management technology found on newer-generation DDR5 DIMMs. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

21. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or

memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

22. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

B. The '087 Patent

23. The '087 Patent is entitled "Memory Package Having Stacked Array Dies and Reduced Driver Load," and was filed on March 14, 2022 and assigned to Netlist, Inc. The '087 Patent issued on May 20, 2025 and claims priority to, among others, U.S. Application No. 13/288,850, filed Nov. 3, 2011, and U.S. Provisional No. 61/409,893, filed November 3, 2010.

24. Claim 1 of the '087 Patent provides:

[1pre] A dynamic random access memory (DRAM) package, comprising:

[1a] stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;

[1b] terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals, wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;

[1c] die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data

interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;

[1d] a control die coupled between the terminals and the stacked DRAM dies, the control die including conduits, the conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;

[1e] wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

[1f] wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;

[1g] wherein a first data interconnect of the first data interconnects is in electrically communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies, each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;

[1h] wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;

[1i] wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;

[1j] wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal;

[1k] wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;

[1l] wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;

[1m] wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;

[1n] wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and

[1o] wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects, and in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

C. The '731 Patent

25. The '731 Patent is entitled "Memory Module And Circuit Providing Load Isolation And Noise Reduction."

26. Claim 1 of the '731 Patent provides:

[1a] A memory module operable to communicate data with a system memory controller via a memory bus in response to address and control signals from the system memory controller, comprising:

[1b] a printed circuit board comprising at least one connector configured to be operatively coupled to the memory bus, the at least one connector including a plurality of edge connections distributed along one or more edges of the printed circuit board;

[1c] a plurality of memory devices on the printed circuit board, the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus;

[1d] at least one circuit coupled between the at least one connector and the plurality of memory devices, the at least one circuit comprising a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices;

[1e] each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections;

[1f] the each correction circuit of the set of correction circuits including at least one programmable impedance matching circuit; and

[1g] control circuitry configured to receive the address and control signals from the system memory controller and to control the plurality of memory devices in response to the address and control signals, wherein the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit based on which of the multiple ranks is

selected to communicate data with the system memory controller in response to the address and control signals.

27. Netlist owns by assignment the entire right, title, and interest in and to the '731 Patent. The '731 Patent was filed as Application No. 14/715,491 on May 18, 2015, issued as a patent on July 17, 2018 and claims priority to, among others, U.S. Application No. 14/324,990, filed on July 7, 2014, Application No. 13/412,243, filed on Mar. 5, 2012, Application No. 12/422,853, filed on Apr. 13, 2009, as well as three provisional applications filed on April 14, 2008 (Nos. 61/044,839, 61/044,825, and 61/044,801).

28. Netlist presented its patented technologies disclosed in the '731 Patent to Micron at least as of February and/or April 2015. Micron had had actual knowledge of the '731 Patent no later than April 28, 2021 via Exhibit A to Netlist's April 28, 2021 letter to Micron, and as of the filing of this First Amended Complaint.

D. Defendants' Infringing Activities

29. Defendants are worldwide semiconductor solution providers that primarily manufacture semiconductor memory products such as DRAM, DIMMs, and MCP (Multi-Chip Package), such as HBM. Defendants develop, manufacture, sell, offer to sell, import into the United States and export from the United States memory components and memory modules (including semi-finished ones) designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications as well as for use in consumer end products.

30. Avnet "is one of the largest distributors of electronic components, computer products and embedded technology." Ex. 15. Avnet has been an official distributor for Micron for more than 40 years, "helping [Micron's] customers to innovate and win." *Id.* As an authorized distributor of Micron memory products, Avnet "accelerates its partners' success by connecting the world's leading technology suppliers with a broad base of customers by providing cost-effective,

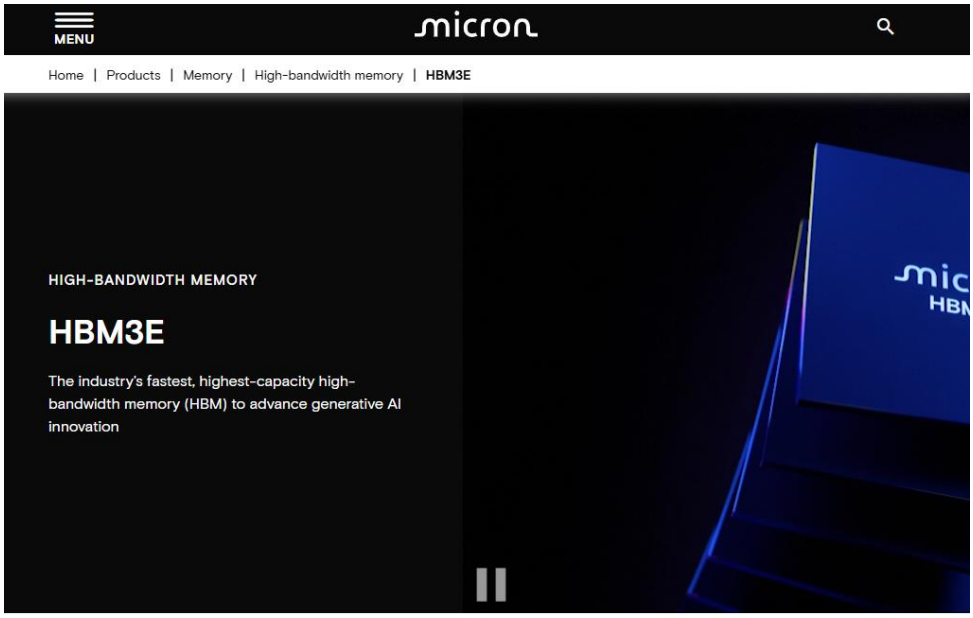
value-added services and solutions." *Id*. Avnet is involved in the use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below (Ex. 13). In addition to offering for sale, selling, and distributing the Accused Instrumentalities as Micron's official distributor, "Avnet and Micron also work cooperatively to train engineers on design techniques to leverage next-generation memory technologies." Ex. 15.

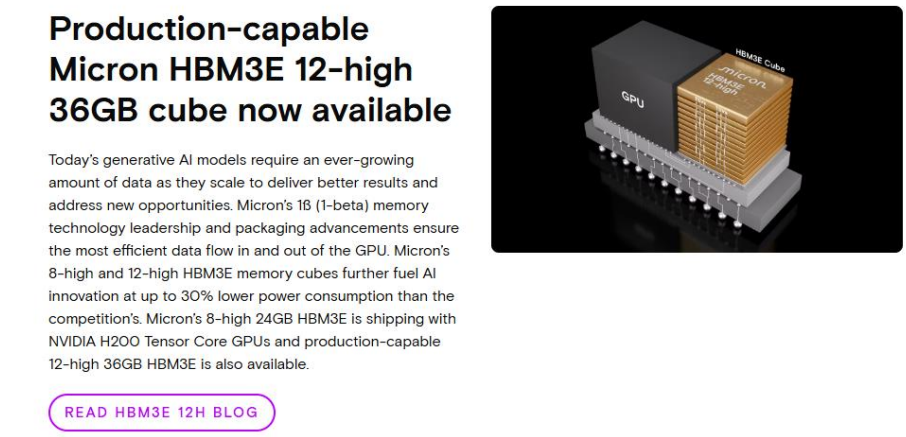
E. High Bandwidth Memory ("HBM")

31. HBM is a type of high-speed computer memory technology that relies in part on vertically-stacked memory dies and differs from the DDR4 or DDR5 DIMM formats described in the paragraphs above. Micron is a major supplier of HBM. Micron itself confirms that "Micron's 8-high and 12-high HBM3E memory cubes further fuel AI innovation at up to 30% lower power consumption than the competition's." https://www.micron.com/products/memory/hbm/hbm3e.

32. The Accused HBM Products include, without limitation, any Micron HBM3E, and newer products (e.g., HBM4; HBM4e[1]) made, sold, used, offered for sale, and/or imported into the United States by Micron. By way of non-limiting example, the accused HBM products include the HBM3E products advertised on Micron's website:

[1] Micron has announced development of HBM4e products in its Financial Results FQ1 2025 Report. ("Development work is well underway with multiple customers on HBM4E.").



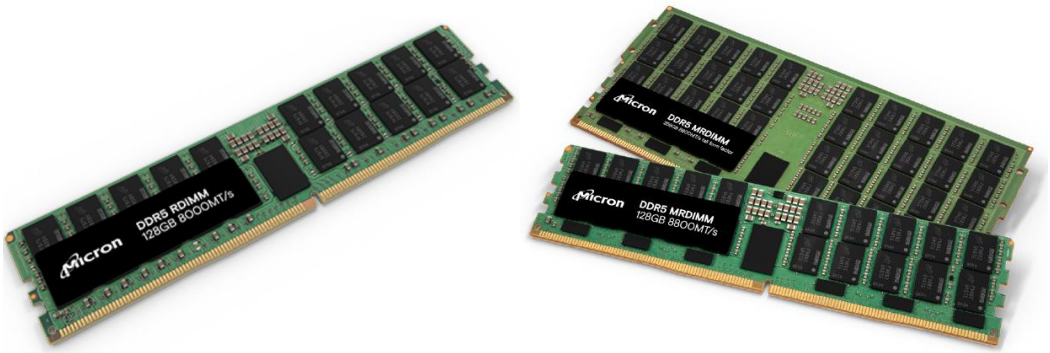


33. On information and belief, the Accused HBM Products are compliant with the applicable memory standards promulgated by the Joint Electron Device Engineering Council ("JEDEC").

F. DDR5 Memory Modules

34. The Accused DDR5 Products include, without limitation, any Micron DDR5 products made, sold, offered for sale, used and/or imported into the United States by Defendants. By way of non-limiting example, the accused DDR5 memory modules with DFE and ODT/RTT circuitry include Micron's DDR5 RDIMMs and MRDIMMs. As further example, the Accused Instrumentalities include, without limitation, any DDR5 products made, sold, offered for sale, used

and/or imported into the United States by Defendants, including those modules utilizing Micron's own power management IC. The Accused DDR5 Products also include any DDR5 products sold, offered for sale, used and/or imported into the United States by Defendants that include PMICs supplied by third parties.



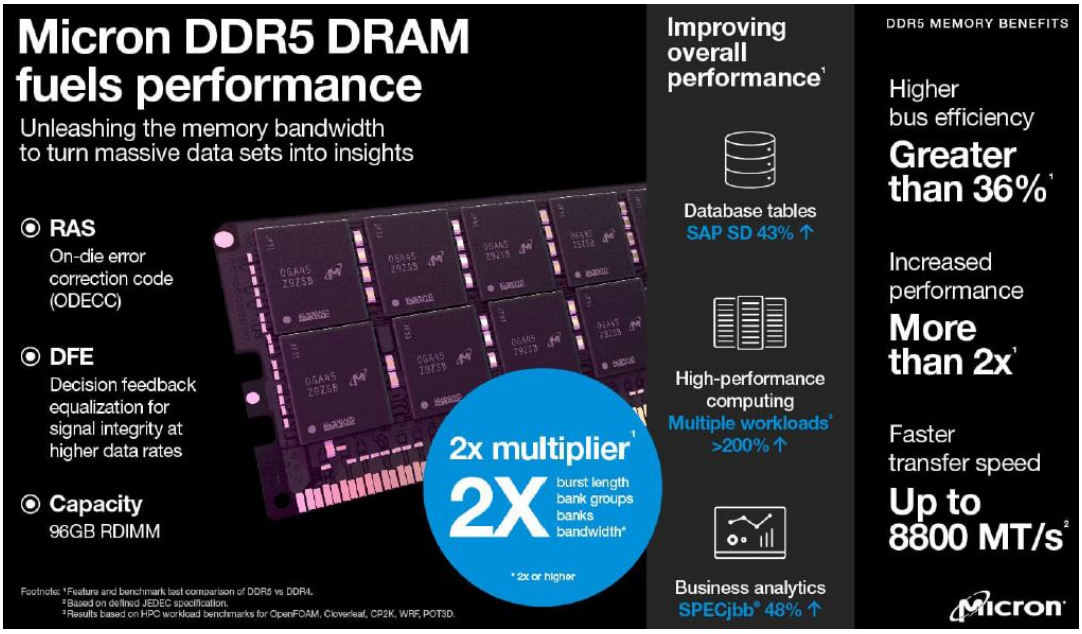
Exs. 3-4 (Micron DDR5 RDIMM and MRDIMM Product Briefs).

35. As seen, each of the DDR5 memory modules includes a plurality of connections at the edge through which command/address signals are received from a memory controller of the host computer system and data is exchanged with the memory controller. Some modules, such as Micron's DDR5 RDIMMs, also include a module controller called "RCD."

36. DDR5 memory modules introduced important upgrades over DDR4 modules. For example, to accommodate higher data rate, DDR5 introduced a feature called "DFE," or Decision Feedback Equalizer, to equalize DQ receivers, which, by providing stable, reliable signal integrity on the module, enables the DQ data eye to open up more, thus enabling higher data rates. Ex. 5 (Micron DDR5 SDRAM Whitepaper), at 3 ("there are critical new features that enable these higher data rates to be achieved. One of these is the addition of equalization in the form of a multi-tap decision feedback equalizer (DFE) in the DQ receivers. The DFE mitigates the effects of inter-symbol interference (ISI) at the higher rates by opening up the data eyes inside the device."); Ex. 9 (Essential Guide to Micron DDR5) ("Decision Feedback Equalization (DFE) was added to improve IO speed scalability and enable high-frequency interfaces. In communications, equalizers

are used to reduce inter-symbol interference (ISI) to allow recovery of the transmitted symbols. ISI is the effect that a given symbol has on the response from subsequent symbols observed at the receiver. DFE is a filter that uses feedback of detected symbols to produce an estimate of the channel output. This is the first time it's been in the DRAM itself.").

37. In conjunction with the DFE feature, DDR5 memory modules optimized on-die termination (ODT) technology to enhance signal integrity. Ex. 6 (DDR5's Secret Weapon: On-Die Termination), 2 ("By placing a termination resistor that matches the transmission line's impedance right on the memory chip, on-die termination minimizes the possibility of signal reflects. Therefore, ODT is a crucial component for high-speed DDR5 memory systems since it aids in enhancing signal quality, decreasing signal ringing, and eventually allowing for higher data transfer speeds with less deterioration."); see also Ex. 8 (Micron DDR5: Client Module Features), at 4 ("DDR5 uses on-die termination (ODT) instead of discrete termination used on DDR4.") ("DDR5 adds the benefit of programmable ODT for CK, CS, and CA, as well as per-device configuration CA_ODT pin.").



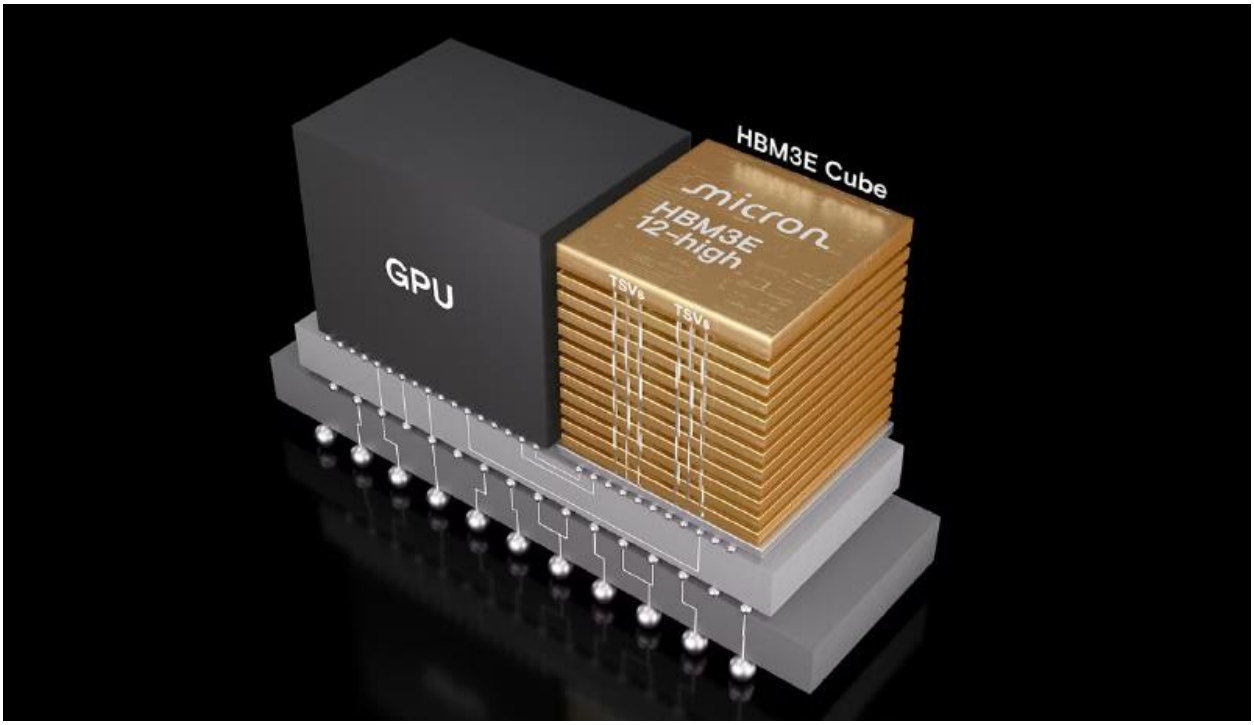
Ex. 10.

IV. FIRST CLAIM FOR RELIEF – '087 Patent

38. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

39. On information and belief, Defendants directly infringed and are currently infringing at least one of the approved claims of the '087 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused HBM Products, and other products with materially the same structure in relevant part. For example, and as shown below, the Accused HBM Products and other products with materially the same structure and operating mechanisms in relevant part infringe at least claim 1 of the '087 Patent.

40. To the extent the preamble is limiting, the Accused HBM Products are a DRAM package. Additionally, as shown below, the Accused HBM Products each include stacked DRAM dies (*e.g.*, 8, 12, or 16 DRAM dies) including at least a first plurality and second plurality of DRAM dies, with each DRAM die of the stacked DRAM dies including C/A ports, data ports, and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells. *See, e.g.*, https://www.micron.com/about/blog/applications/ai/microns-hbm3e-powering-the-future-of-ai-with-high-bandwidth-memory ("HBM3E is highly energy-efficient because the data path between the host and memory is shorter. The DRAM communicates with the host through silicon vias or TSVs, which Girish explains as being similar to a toothpick through a burger. It takes power and data from the bottom die and moves it to the top memory layer. Micron's HBM3E consumes 30% less power than the competition because of the advanced CMOS technology innovation on the 1β process node and advanced packaging innovations with up to 2 times TSVs coupled with 25% shrink in package interconnects.").



41. The Accused HBM Products also include terminals with command and/or address (C/A) terminals and data terminals, via which the memory package communicates, e.g., control/address signals and data signals in response to the C/A signals, respectively. For example, the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a memory read operation, and to receive second data signals in response to a second set of C/A signals associated with a memory write operation. To illustrate, JEDEC Standard No. 238A provides the following Command Truth Table listing the command and/or address signals associated with a memory read operation and memory write operation:

6.3.1 Command Truth Tables (cont'd)

Table 31 — Column Commands Truth Table

Command [4]	Symbol	Clock Cycle	C0	C1	C2	C3	C4	C5	C6	C7	Notes
Column No Operation	CNOP	R	H	H	H	V	V	V	V	V	1, 2, 3
		F	V	V	V	V	V	V	V	V	
Read	RD	R	H	L	H	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Read w/ AP	RDA	R	H	L	H	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6, 7
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write	WR	R	H	L	L	L	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Write w/ AP	WRA	R	H	L	L	H	PC	SID0 / V	SID1 / V	BA0	1, 2, 3, 5, 6
		F	BA1	BA2	BA3	CA0	CA1	CA2	CA3	CA4	
Mode Register Set	MRS	R	L	L	L	MA4	OP5	OP6	OP7	MA0	1, 3, 8, 9
		F	MA1	MA2	MA3	OP0	OP1	OP2	OP3	OP4	

NOTE 1 BA = Bank Address; CA = Column Address; PC = Pseudo Channel 0 or 1; SID = Stack ID; MA = Mode Register Address; V = Valid Signal (either H or L, but not floating).

NOTE 2 C[7:0] must be driven to a valid signal level even if a stack ID address (SID) is not defined for a specific density, or if parity is disabled in the mode register. APAR must be driven to a valid signal level even if CA parity is disabled in MR0 OP6. C[7:0] are Don't Care when the device is in power-down or self refresh.

NOTE 3 Parity is evaluated on all pins if CA parity is enabled in MR0 OP6.

NOTE 4 All other command encodings not shown in the table are reserved for future use.

NOTE 5 PC = 0 selects pseudo channel 0 (PC0), and PC = 1 selects pseudo channel 1 (PC1). The pseudo channel not selected by PC performs a CNOP.

NOTE 6 The SID bits act as bank address bits in conjunction with READ and WRITE commands, and related timing diagrams shall be interpreted accordingly. All other column commands do not use SID. Refer to the channel addressing table for HBM3 configurations using SID.

NOTE 7 HBM3 configurations using the SID specify a timing parameter t_{CCDR} for consecutive READs to different SID. Vendor datasheets should be consulted for details.

NOTE 8 All mode registers are write-only by default using the MRS command.

NOTE 9 Refer to the HBM3 Mode Register Overview table for MA4 of MRS.

42. The Accused HBM Products further include die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects configured to conduct the first data signals and the second data signals, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked array dies through the one or more TSVs. *See*

https://www.micron.com/about/blog/applications/ai/microns-hbm3e-powering-the-future-of-ai-with-high-bandwidth-memory; *see also* Micron HBM3E Product Brief.

43. As shown above, the Accused HBM Products also include a control die (also known as a "buffer die" or "logic die") coupled between the terminals and the stacked DRAM dies. *See also, e.g.*, Micron Fiscal Q4 2023 Earnings Call Prepared Remarks at 6 ("The HBM product includes a logic interface die . . . ."). The control die includes conduits including C/A conduits and data conduits, the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects, the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects.

44. The Accused HBM Products also have C/A interconnects in the claimed configuration. For example, a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not with any C/A port on any of the second plurality of DRAM dies. Similarly, a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not with any C/A port on any of the first plurality of DRAM dies.

45. The Accused HBM Products also have data interconnects in the claimed configuration. For example, a first data interconnect of the first data interconnects are in electrical communication with data ports on the first plurality of DRAM dies and not with any data port on any of the second plurality of DRAM dies. Further, each of the first data interconnects includes a first respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies, wherein

the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die. Similarly, a second data interconnect of the second data interconnects is in electrical communication with data ports on the second plurality of DRAM dies and not with any data port on any of the first plurality of DRAM die. For example, as depicted above, some TSVs appear to only electrically interconnect to some of the dies in the stack, while others may electrically bypass certain groups of dies.

46. Additionally, the data conduits in the control die include a first conduit of the first data conduits coupled between the first data interconnect and a first data terminal of the data terminals (e.g., one or more data terminals), and a second conduit of the second data conduits coupled between the second data interconnect and the first data terminal (e.g., one or more data terminals). The control die also includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal (e.g., as shown above in the Command Truth Table of JESD 238A).

47. The Accused HBM Products further include first and second unidirectional die interconnects, for example, respective TSVs associated with unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c. *See, e.g.*, JESD 238A ("Data referenced to unidirectional differential data strobes RDQS_t/RDQS_c and WDQS_t/WDQS_c."); *id.* (reproduced below). For example, the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects (*e.g.*, RDQS_t/RDQS_c in response to the first set of C/A signals) and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects. As further

example, the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects (e.g., WDQS_t/WDQS_c in response to the second set of C/A signals) and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects.

6 Operation

6.1 HBM3 Clocking Overview

The HBM device captures commands and addresses on the row and column buses using a differential clock CK_t/CK_c. Both buses operate at double data rate (DDR).

The HBM device has uni-directional differential Write strobes (WDQS_t/WDQS_c) and Read strobes (RDQS_t/RDQS_c) per 32DQ(DWORD). The data bus operates at double data rate (DDR).

HBM3 utilizes two types of clock with different frequencies. The strobe frequency is twice the frequency of the command clock, requiring an HBM3 to have reset-type clock-divider in the WDQS clock tree (Figure 10). By dividing the WDQS, the operation speed of DRAM internal circuits in WDQS domain is reduced to half. The direction of the internal WDQS/2 transition may vary depending on vendor's choice. Command clock and WDQS are generated from the same PLL and RDQS clock is generated from WDQS. WDQS internal divider is initialized to be a pre-defined internal divider state after Self Refresh exit or Power-up or Power down exit sequence. The sum of preamble and postamble for both READ and WRITE operation is required to be an even number so that the internal divider's state, phase of internal WDQS/2, is maintained. Therefore, HBM3 WDQS does not require a specific sync operation before READ and WRITE operations. WDQS starts toggling before starting WRITE or READ operations for reducing ISI. During inactivity, WDQS/ RDQS are required to be static (WDQS/RDQS_t is Low, WDQS/RDQS_c is High). When WRITE training for unmatched DQ/DQS path, DQ should be shifted to align phase to the point where CK and WDQS are in sync.

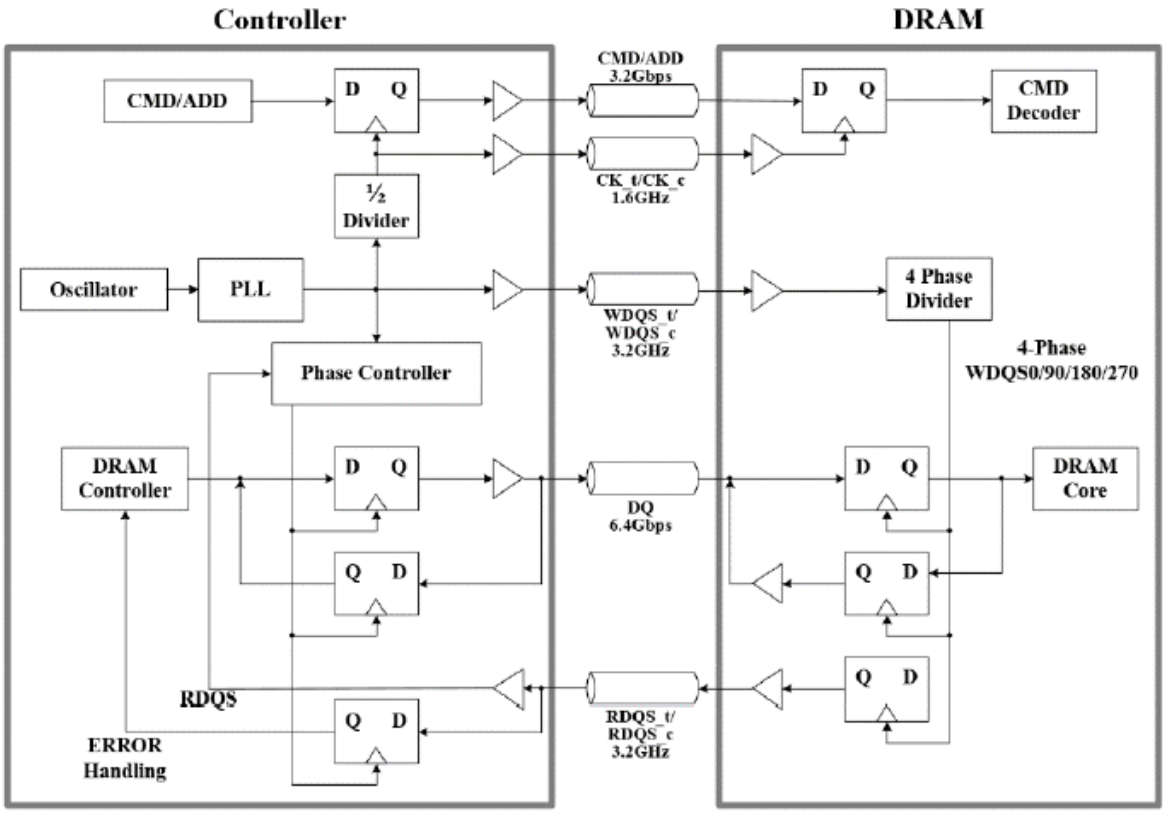


Figure 10 — High Level Block Diagram Example of Clocking Scheme

48. On information and belief, Micron also indirectly infringes the ’087 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Micron’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has induced, and currently induces, the infringement of the ’087 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the Accused HBM Products and other materially similar products that infringe the ’087 Patent. On information and belief, Micron provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the Accused HBM Products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement. On information and belief, Micron is encouraging and facilitating infringement of the ’087 Patent by others. For example, on information and belief, Micron sells or otherwise provides the Accused HBM Products to

distributors or U.S.-based sales entities knowing that these entities intend to make, use, offer to sell, and/or sell the products within the United States and/or import the products into the United States in an infringing manner.

49. On information and belief, Micron also indirectly infringes the '087 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Micron has contributed to, and currently contributes to, Micron's customers and end-users infringement of the '087 Patent through its affirmative acts of selling and offering to sell, either directly or through its distributors, in this District and elsewhere in the United States, the Accused HBM Products and other materially similar products that infringe the '087 Patent. On information and belief, the Accused HBM Products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Micron is aware that the product or process that includes the Accused HBM Products and other materially similar products may be covered by one or more claims of the '087 Patent. On information and belief, the use of the product or process that includes the Accused HBM Products and other materially similar products infringes at least one claim of the '087 Patent.

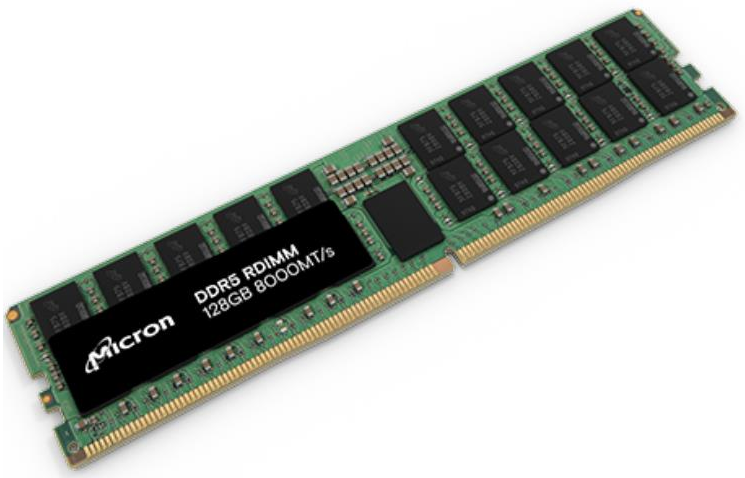
50. Micron's infringement of the '087 Patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '087 Patent since at least the filing of the original Complaint. Micron's infringement of the '087 Patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

V. SECOND CLAIM FOR RELIEF – '731 Patent

51. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this First Amended Complaint as if fully set forth herein.

52. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '731 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 DIMMs with DFE and ODT/RTT circuitry, such as RDIMMs and MRDIMMs, and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR5 RDIMMs and other products with materially the same structures in relevant parts infringe at least one claim of the '731 Patent.

53. For example, the accused DDR5 RDIMMs are memory modules "operable to communicate data with a system memory controller via a memory bus in response to address and control signals from the system memory controller" and comprise "a printed circuit board comprising at least one connector configured to be operatively coupled to the memory bus, the at least one connector including a plurality of edge connections distributed along one or more edges of the printed circuit board":



Ex. 3, at 1.

54. As shown above and below, the accused DDR5 RDIMMs comprise "a plurality of memory devices on the printed circuit board," e.g., Micron DDR5 SDRAMs arranged in multiple ranks ("the plurality of memory devices being arranged in multiple ranks, each rank comprising an independent set of memory devices that can be accessed by the system memory controller to access a full bit-width of the memory bus"):

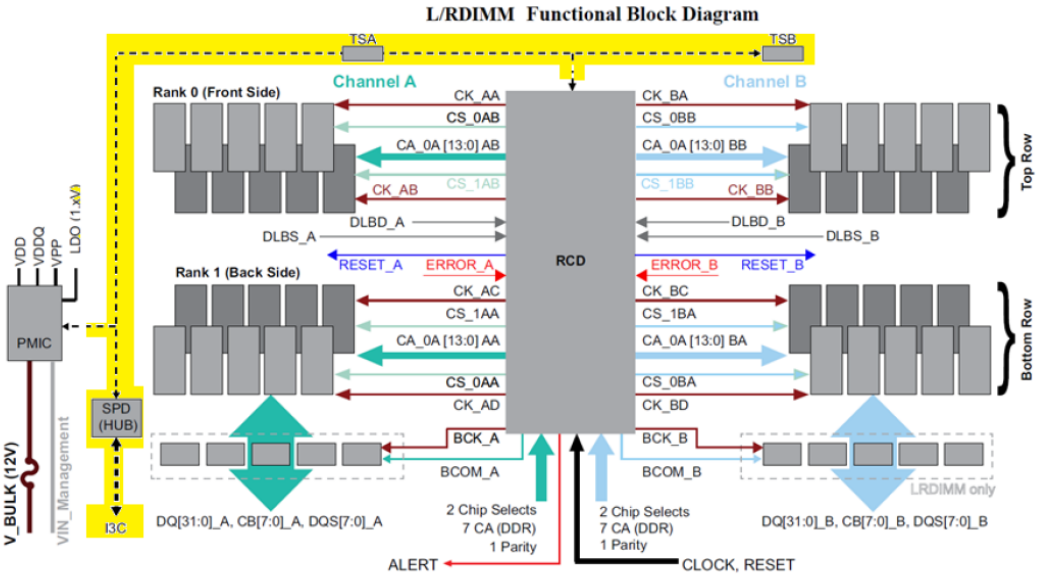
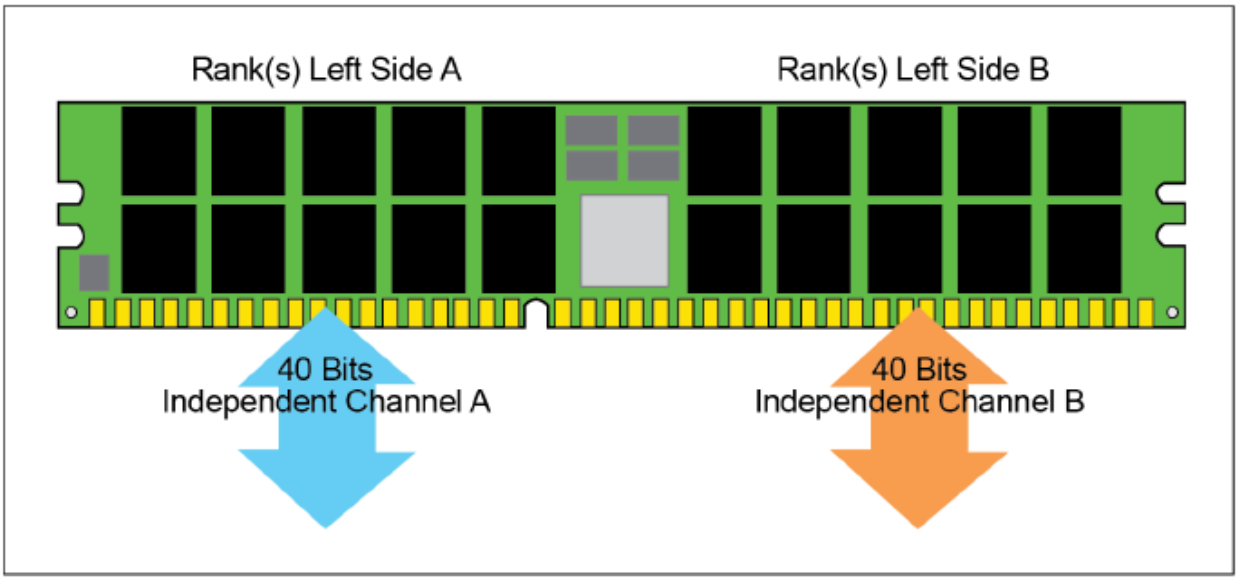


Figure 2: Functional Block Diagram of RDIMM and LRDIMM Memory

Ex. 7, at 1.



Ex. 5, at 4.

55. By way of further example, the accused DDR5 RDIMMs comprise "at least one circuit coupled between the at least one connector and the plurality of memory devices, the at least one circuit comprising a first set of port connections coupled to respective ones of the plurality of edge connections and a second set of port connections coupled to the plurality of memory devices, each circuit of the at least one circuit further comprising a set of correction circuits, each correction circuit of the set of correction circuits being configured to make corrections in one or more signals transmitted between a respective port connection of the first set of port connections and a corresponding port connection in the second set of port connections, the each correction circuit of the set of correction circuits including at least one programmable impedance matching circuit":

Decision Feedback Equalization

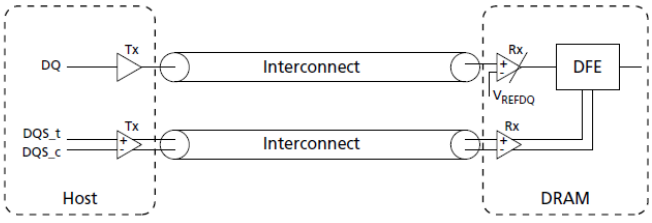
At data rates ≥2933 MT/s, signal degradation due to inter symbol interference (ISI) is expected to increase and the data eye at the device ball is expected to be closed. Because the memory channel is very reflective due to the many impedance mismatched points that exist along the memory subsystem, ISI due to reflections is expected to increase.

Traditional methods of characterizing the receiver using the input eye mask are no longer sufficient. DDR5 requires equalization to help improve (or open up) the data eyes after data is latched by the receiver. A 4-tap decision feedback equalization (DFE) helps equalize the DQ signals without amplifying the noise due to insertion loss and reflections, which is a common side effect of other equalization techniques (for example, CTLE). For ISI correction to occur, the Global DFE Gain and Tap (MR111) and per-pin DFE Gain and Tap (MR112-MR252) bits shall be enabled and properly configured for data rates ≥ 2933 MT/s. When the DFE is enabled, the DQs shall be high for a minimum of 4UI prior to the first write data bit to ensure proper DFE synchronization.

The figure below shows an example of a memory subsystem with DFE circuit included on the device.

For systems supporting data channel margins where the DFE is not required to improve signaling, the DFE can be disabled. Also, at the 1980-2100 MT/s data rates, the device's DFE is disabled. Setting either the global DFE gain and tap 1-4 enable bits to disable or setting all DFE gain and tap 1-4 bias bits to step 0 disables the DFE.

Figure 158: Memory Subsystem with DFE Circuit on the Device



Ex. 11 (Micron DDR5 SDRAM Product Core Datasheet), at p. 275

16Gb DDR5 SDRAM Addendum

MT60B4G4, MT60B2G8, MT60B1G16
Die Revision A

Features

This document describes the product specifications that are unique to Micron 16Gb DDR5 Die Revision A device. For general Micron DDR5 SDRAM specifications, see the Micron DDR5 SDRAM Core Product Data Sheet. Content in this 16Gb Die Revision A DDR5 SDRAM data sheet addendum supersedes content defined in the core data sheet.

- $V_{DD} = V_{DDQ}$ = 1.1V (NOM)
- V_{PP}= 1.8V (NOM)
- On-die, internal, adjustable V_{REF} generation for DQ, CA, CS
- 1.1V pseudo open-drain I/O
- TC maximum up to 95°C
  - 32ms, 8192-cycle refresh up to 85°C
  - 16ms, 8192-cycle refresh at >85°C to 95°C
- 32 internal banks (x4, x8): 8 groups of 4 banks each
- 16 internal banks (x16): 4 groups of 4 banks each
- 16n-bit prefetch architecture
- 1 cycle/2 cycle command structure
- 2N mode
- All bank and same bank refresh
- Multi-purpose command (MPC)
- CS/CA training mode
- On-die ECC (bounded fault)
- ECC transparency and error scrub
- Decision feedback equalization (DFE)
- Loopback mode
- Command-based non-target (NT) nominal, DQ/DQS park, and dynamic WR on-die termination (ODT)
- sPPR and hPPR capability
- Per-DRAM addressability
- JEDEC JESD-79.5 compliant

Options[1]	Marking
• Configuration	
– 4 Gig x 4	4G4
– 2 Gig x 8	2G8
– 1 Gig x 16	1G16
• FBGA SDP Packages (Pb-free)	
– x4, x8 82-ball (9mm x 11mm)	HB
– x16 102-ball (9mm x 14mm)	HC
• Timing – cycle time	
– 0.416ns @ CL = 40	-48B
• Operating temperature	
– Commercial (0°C < T_C < 95°C)	None
– Industrial (–40°C < T_C < 95°C)	IT
– Automotive (–40°C < T_C < 105°C)	AT
• Die Revision	:A

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on micron.com for available offerings.

Ex. 12 (Micron 16Gb DDR5 SDRAM Addendum Datasheet), at 1.

On-Die Termination

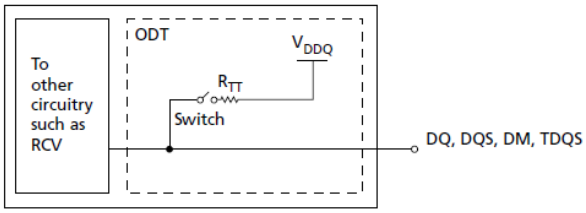
On-Die Termination for DQ, DQs, DM and TDS

On-die termination (ODT) enables the DRAM to change termination resistance for each DQ, DQS, DM and TDQS pin. Unlike previous DDR technologies, DDR5 no longer has a physical ODT pin, and all ODT-based control is now command- and mode register-based. For x4 and x8 configuration devices, ODT is applied to each DQ, DQS_t, DQS_c and DM_n, as well as TDQS_t, TDQS_c for x8 configuration). For x16 configuration devices, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n. ODT is enabled via non-target READ/MODE REGISTER READ commands, WRITE and NON-TARGET WRITE commands, or is set to the default PARK value through settings in MR33-MR35.

The ODT feature is designed to improve signal integrity of the memory channel by enabling the device controller to independently change termination resistance for any or all devices. In addition to the control capability of the DQ ODT, the DQS ODT is now independently programmed via MR33:OP[5:3] and held static. All ODT control is targeted for the DQs. This addition enables adjusting the delay common in an unmatched architecture. DQS RTT offset control mode is enabled via MR40:OP[2:0].

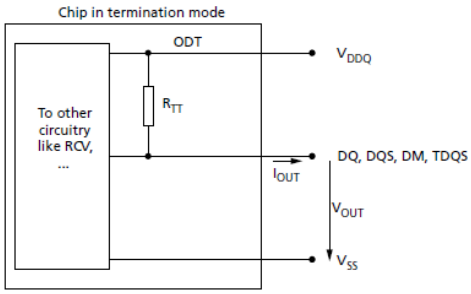
The ODT feature is turned off and not supported in self refresh mode, but does have an optional mode when in power-down. The figure below shows a simple functional representation of the ODT feature.

Figure 201: Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses command decode, mode register settings and other control information (see below). The value of RTT is determined by the settings of mode register bits.

Figure 202: On Die Termination



Note: 1. Supported on die termination effective RTT values are: 240, 120, 80, 60, 48, 40, 34 ohms.

Ex. 11 (Micron DDR5 SDRAM Product Core Datasheet), at 328. On information and belief, the DFE and ODT circuit are not part of the memory device.

Table 274: ODT Electrical Characteristics R_{ZQ} = 240Ω +/- 1% Entire Temperature Range, After Proper ZQ Calibration

RTT	V_{OUT}	MIN	Nom	MAX	Unit	Notes
240Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	R_{ZQ}	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	R_{ZQ}	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	R_{ZQ}	1,2,3
120Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/2$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/2$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/2$	1,2,3
80Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/3$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/3$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/3$	1,2,3
60Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/4$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/4$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/4$	1,2,3
48Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/5$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/5$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/5$	1,2,3
40Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/6$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/6$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/6$	1,2,3
34Ω	V_{OLdc} = 0.5* V_{DDQ}	0.9	1	1.25	$R_{ZQ}/7$	1,2,3
	V_{OMdc} = 0.8* V_{DDQ}	0.9	1	1.1	$R_{ZQ}/7$	1,2,3
	V_{OHdc} = 0.95* V_{DDQ}	0.8	1	1.1	$R_{ZQ}/7$	1,2,3
DQ-DQ mismatch within byte	V_{OMdc} = 0.8* V_{DDQ}	0	–	8	%	1,2,4,5,6

Ex. 11 (Micron DDR5 SDRAM Product Core Datasheet), at 329.

MR34 RTT_PARK and RTT_WR

Table 55: MR34 Register and OP-Code Bit Definitions (MA[7:0] = 22h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU		RTT_WR			RTT_PARK		

Function	Type	OP	Description/Data	Notes
RTT_PARK	R	OP[2:0]	000b=RTT_OFF (default), 001b=R_{ZQ} (240 ohm), 010b=R_{ZQ}/2(120 ohm), 011b=R_{ZQ}/3 (80 ohm), 100b=R_{ZQ}/4 (60 ohm), 101b= R_{ZQ}/5 (48 ohm), 110b=R_{ZQ}/6 (40 ohm), 111b= R_{ZQ}/7 (34 ohm)	1
RTT_WR	R/W	OP[5:3]	000b=RTT_OFF, 001b=R_{ZQ} (240 ohm) (default), 010b=R_{ZQ}/2 (120 ohm), 011b=R_{ZQ}/3 (80 ohm), 100b=R_{ZQ}/4 (60 ohm), 101b= R_{ZQ}/5 (48 ohm), 110b=R_{ZQ}/6 (40 ohm), 111b= R_{ZQ}/7 (34 ohm)	
RFU	RFU	OP[7:6]	RFU	

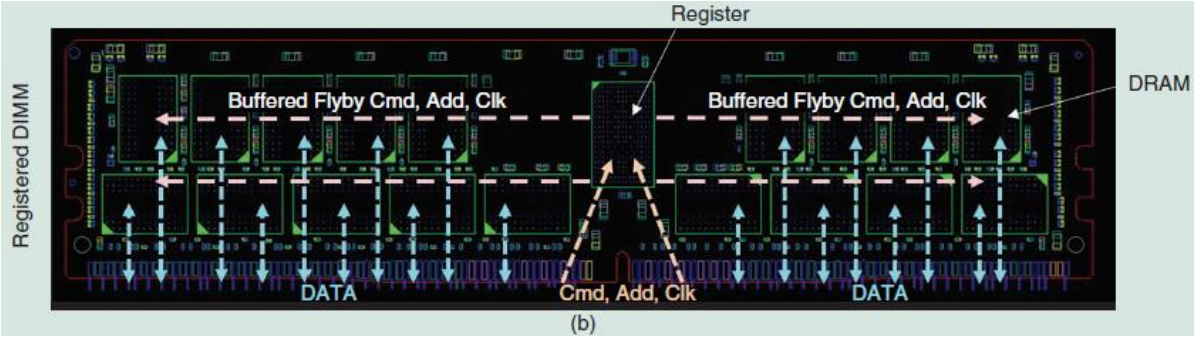
Note: 1. This mode register is programmed via an explicit MPC command only.

Ex. 11 (Micron DDR5 SDRAM Product Core Datasheet), at 76.

56. Each "DDR5 device" on the memory module includes a memory device comprising memory cores and the at least circuitry such as DDR5-specific DFE and ODT/RTT circuits, which is each a correction circuit including at least one programmable impedance matching circuit. The collection of the DFE and ODT/RTT circuits forms a set of correction circuits. Each DFE and ODT/RTT circuit associated with a DQ line is configured to make corrections in one or more DQ signals transmitted between a respective port connection (*e.g.*, one for a data or DQ signal line) of the first set of port connections connected to the edge connector and a corresponding port connection for a DDR5 memory device in the second set of port connections.

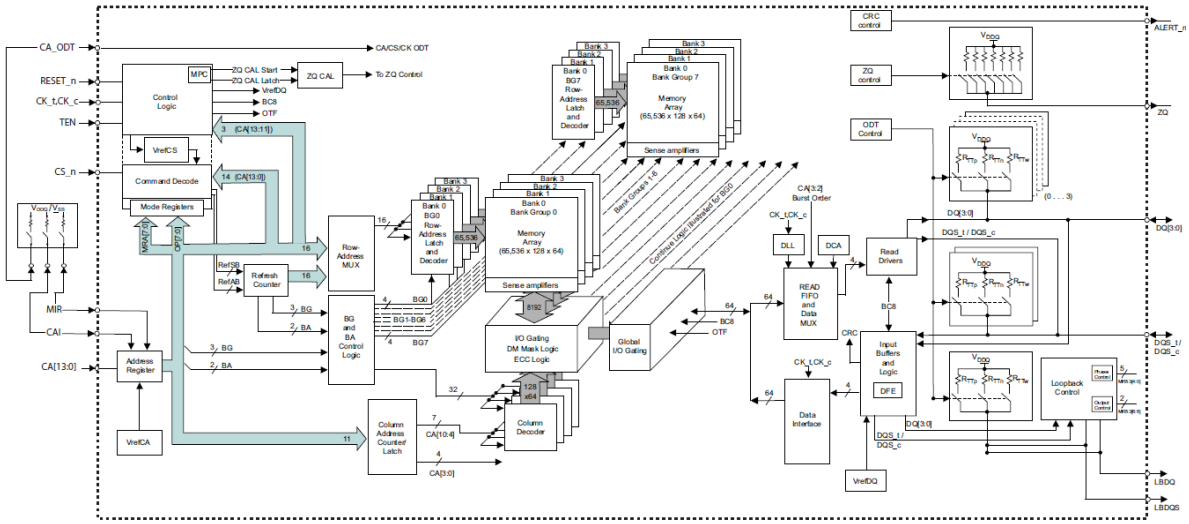
57. By way of further example, as shown above and below, the accused DDR5 RDIMMs comprise "control circuitry" "configured to receive the address and control signals from the system memory controller and to control the plurality of memory devices in response to the address and control signals, wherein the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit in the each correction circuit of the set of correction circuits in the each circuit of the at least one circuit based on which of the multiple ranks is selected to communicate data with the system memory controller in response to the address and control signals." For example, on information and belief, the control circuitry is configured to receive the address and control signals from the memory controller and to output

appropriate address and control signals based on the received address and control signals for controlling the plurality of memory devices in response to the address and control signals received from the system memory controller, as shown below:



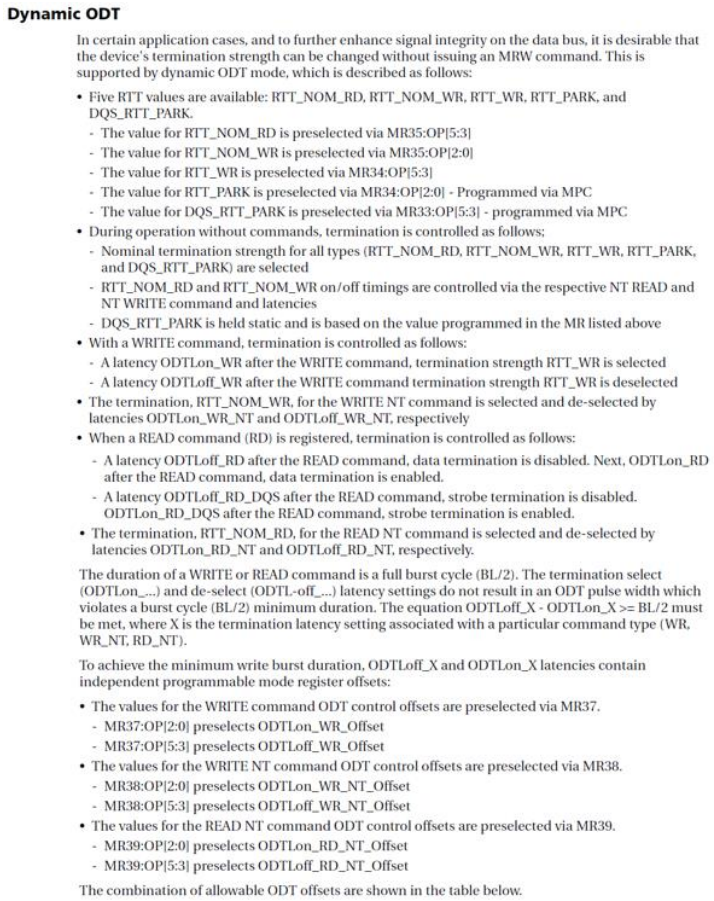
Ex. 14 (Recent Evolution in the DRAM Interface: Mile-Markers Along Memory Lane), at 18-19 ("In a later effort to shorten and simplify the overall command/address/control and clock signal paths, a register was introduced on the registered DIMM to intercept and retransmit those signals out to the DRAMs, resulting in a substantial signal margin increase at each DRAM location").

Figure 2: 4 Gig x4 Functional Block Diagram



Ex. 12 (Micron 16Gb DDR5 SDRAM Addendum Datasheet), at 5; *see also id* at 6. By further example, on information and belief, the control circuitry is further configured to dynamically control the at least one programmable impedance matching circuit (ODT/RTT) of the set of correction circuits because the RTT value of the targeted rank is set based on the address and

control signal received, such as the chip select signals that determine the ranks to be accessed and that in DDR5 encodes the ODT signal.



Dynamic ODT

In certain application cases, and to further enhance signal integrity on the data bus, it is desirable that the device's termination strength can be changed without issuing an MRW command. This is supported by dynamic ODT mode, which is described as follows:

- Five RTT values are available: RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK.
  - The value for RTT_NOM_RD is preselected via MR35:OP[5:3]
  - The value for RTT_NOM_WR is preselected via MR35:OP[2:0]
  - The value for RTT_WR is preselected via MR34:OP[5:3]
  - The value for RTT_PARK is preselected via MR34:OP[2:0] - Programmed via MPC
  - The value for DQS_RTT_PARK is preselected via MR33:OP[5:3] - programmed via MPC
- During operation without commands, termination is controlled as follows;
  - Nominal termination strength for all types (RTT_NOM_RD, RTT_NOM_WR, RTT_WR, RTT_PARK, and DQS_RTT_PARK) are selected
  - RTT_NOM_RD and RTT_NOM_WR on/off timings are controlled via the respective NT READ and NT WRITE command and latencies
  - DQS_RTT_PARK is held static and is based on the value programmed in the MR listed above
- With a WRITE command, termination is controlled as follows:
  - A latency ODTLon_WR after the WRITE command, termination strength RTT_WR is selected
  - A latency ODTLoff_WR after the WRITE command termination strength RTT_WR is deselected
- The termination, RTT_NOM_WR, for the WRITE NT command is selected and de-selected by latencies ODTLon_WR_NT and ODTLoff_WR_NT, respectively
- When a READ command (RD) is registered, termination is controlled as follows:
  - A latency ODTLoff_RD after the READ command, data termination is disabled. Next, ODTLon_RD after the READ command, data termination is enabled.
  - A latency ODTLoff_RD_DQS after the READ command, strobe termination is disabled. ODTLon_RD_DQS after the READ command, strobe termination is enabled.
- The termination, RTT_NOM_RD, for the READ NT command is selected and de-selected by latencies ODTLon_RD_NT and ODTLoff_RD_NT, respectively.

The duration of a WRITE or READ command is a full burst cycle (BL/2). The termination select (ODTLon_...) and de-select (ODTL-off_...) latency settings do not result in an ODT pulse width which violates a burst cycle (BL/2) minimum duration. The equation ODTLoff_X - ODTLon_X >= BL/2 must be met, where X is the termination latency setting associated with a particular command type (WR, WR_NT, RD_NT).

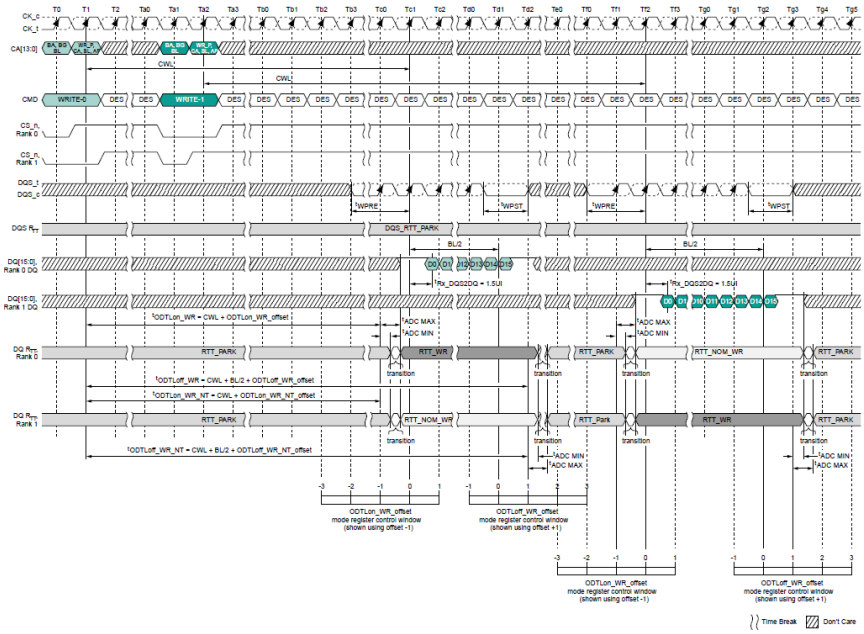
To achieve the minimum write burst duration, ODTLoff_X and ODTLon_X latencies contain independent programmable mode register offsets:

- The values for the WRITE command ODT control offsets are preselected via MR37.
  - MR37:OP[2:0] preselects ODTLon_WR_Offset
  - MR37:OP[5:3] preselects ODTLoff_WR_Offset
- The values for the WRITE NT command ODT control offsets are preselected via MR38.
  - MR38:OP[2:0] preselects ODTLon_WR_NT_Offset
  - MR38:OP[5:3] preselects ODTLoff_WR_NT_Offset
- The values for the READ NT command ODT control offsets are preselected via MR39.
  - MR39:OP[2:0] preselects ODTLon_RD_NT_Offset
  - MR39:OP[5:3] preselects ODTLoff_RD_NT_Offset

The combination of allowable ODT offsets are shown in the table below.

Ex. 11(Micron DDR5 SDRAM Product Core Datasheet), at 331-32.

Figure 209: Example of WRITE to WRITE Turn Around, Different Ranks



Notes: 1. ODTLon_WR, ODTLon_WR_NT, ODTLoff_WR and ODTLoff_WR_NT are based on mode register settings that can push out or pull in the RTT enable and disable time.
2. For simplicity, the entire range of ODTL control is not shown.

Ex. 11 (Micron DDR5 SDRAM Product Core Datasheet), at 340; *see also id.* at 345. The control circuitry receives address and control signals from the memory controller, processes the input address and control signals to appropriate output command/signals (including converting double rated input command/address signals to single rated signals as needed and converting input chip selects to appropriate outputs), and outputs the converted address and control signals to the DDR5 devices.

58. On information and belief, Defendants also indirectly infringe the ’731 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Defendants’ customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Defendants have induced, and currently induce, the infringement of the ’731 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR5 products and other materially similar products that infringe the ’731 Patent. On information and belief, Defendants provide specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the

accused DDR5 memory modules and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement. On information and belief, Micron is encouraging and facilitating infringement of the '731 Patent by others. For example, on information and belief, Micron sells or otherwise provides the Accused Products to distributors or U.S.-based sales entities, including but not limited to, Avnet, knowing that these entities intend to make, use, offer to sell, and/or sell the products within the United States and/or import the products into the United States in an infringing manner. Ex. 13.

59. On information and belief, Defendants also indirectly infringe the '731 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Defendants have contributed to, and currently contribute to, Defendants' customers and end-users infringement of the '731 Patent through its affirmative acts of selling and offering to sell, either directly or through its distributors, in this District and elsewhere in the United States, the accused DDR5 memory modules and other materially similar products that infringe the '731 Patent. On information and belief, the accused DDR5 products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Defendants are aware that the product or process that includes the accused DDR5 products and other materially similar products may be covered by one or more claims of the '731 Patent. On information and belief, the use of the product or process that includes the accused DDR5 products and other materially similar products infringes at least one claim of the '731 Patent.

60. Micron's infringement of the '731 Patent has damaged and will continue to damage Netlist. Micron has had actual notice of the '731 Patent since at least April 28, 2021. Micron's

infringement of the '731 Patent has been continuing and willful. Micron continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Micron knew or should have known that its actions constituted an unjustifiably high risk of infringement.

61. Avnet's infringement of the '731 Patent has damaged and will continue to damage Netlist. Avnet has had actual notice of the '731 Patent at least as early as the filing of this First Amended Complaint. Avnet's infringement of the '731 Patent has been continuing and willful. Avnet continues to commit acts of infringement, including advertising, marketing, offering to sell and/or selling the Accused Products, despite a high likelihood that its actions constitute infringement, and Avnet knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VI. THIRD CLAIM FOR RELIEF

62. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

63. Netlist has not violated Idaho Code § 48-1703 by asserting the Patents-in-Suit against Micron.

VII. DEMAND FOR JURY TRIAL

64. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

VIII. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Defendants infringe the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Defendants' infringement;

C. an award of damages resulting from Defendants acts of infringement in accordance with 35 U.S.C. § 284;

D. that Micron's infringement of the Patents-in-Suit is willful;

E. that Avnet's infringement of the '731 Patent is willful;

F. enhanced damages pursuant to 35 U.S.C. § 284;

G. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

H. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

I. a declaration that Netlist has not made a bad-faith assertion of patent infringement against Micron nor engaged in any unlawful, unfair, or deceptive act or practice in trade or commerce under the Idaho Consumer Protection Act, and is therefore compliant with Idaho Code § 48-1703;

J. a judgment that Micron is not entitled to any award of damages in the pursuit of this litigation pursuant to Idaho Code § 48-1706(b) and (d), § 48-1706(1)(c), Idaho Rule of Civil Procedure 54, and such other and additional provisions of the Idaho Rules of Civil Procedure and Idaho Code, or any other applicable authority;

K. in the alternative to an award of damages under 35 U.S.C. § 284, an order pursuant to 35 U.S.C. § 283 permanently enjoining Defendants, its distributors, officers, agents, servants, employees, attorneys, instrumentalities and those persons in privity, active concert or participation with them, from further acts of direct and/or indirect infringement of the Patents-in-Suit including the manufacture, sale, offer for sale, importation and use of the infringing products.

L. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: July 8, 2025

Respectfully submitted,

/s/ Samuel F. Baxter

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